REMARKS

I. Formal Matters.

Subsequent to entry of the foregoing amendments, claims 1-18 are currently pending in this application. New claims 12-18 are hereby added.

As an initial matter, Applicant thanks the Examiner for acknowledging Applicant's claim to priority under 35 U.S.C. §119 and for confirming receipt of a certified copy of Applicant's foreign priority document. Applicant also thanks the Examiner for indicating that the drawings filed with the subject application papers on September 22, 2003, are acceptable.

II. 35 U.S.C. §102(b).

The Examiner rejects claims 1, 3, 7 and 8 under 35 U.S.C. §102(b) as allegedly being anticipated by *Hwang, et al.* (U.S. Patent No. 6,346,838) (*"Hwang"*). Applicant respectfully traverses this rejection in view of the following remarks.

Claim 1. *Hwang* discloses a variable delay/phase difference being added to both the reference clock (DLL input) and the synchronous clock output of the PLL (*Hwang* Fig. 3). More particularly, voltage controlled delay line (VCDL) 36 adds a variable delay D to the reference clock and VCDL 34 adds variable delay D to the synchronous clock output of the PLL (*Hwang* col. 3, lines 20-51; Fig. 3).

One of these variably delayed signals, FB is then also delayed by a "Fixed delay" in the DLL (*Hwang* Fig. 3; FCK; col. 3, lines 21-26; FCK) *Hwang*'s DLL outputs are designated RCK and FCK, reference and feedback, respectively (*Hwang* Figs. 3 and 4; col. 3, lines 53-57; and col. 4, lines 4-18). Further, the PLL disclosed in *Hwang* receives RCK and FCK as inputs (Fig. 3; col. 3, lines 65-66).

Hwang teaches that "[t]he desired result is that the signals FB and REF are exactly in phase, with the phase being canceled" (col. 3, lines 61-64). Further, "[t]he FB signal is adjusted to be in phase with the REF signal by first detecting their phase difference (with the PFD 38), using a charge pump and...capacitor to produce a control voltage for VCDL 34 [and VCDL 36], such that FB can be in phase with REF (col. 4, lines 37-44). Finally, *Hwang* teaches, "[u]sing a bang-bang type phase detector...the skew (phase offset) between RCK and FCK can be reduced to...almost zero"(col. 5, lines 50-56).

In contrast, claim 1 requires a DLL having "...a phase changing means *for increasing the phase difference* between the reference clock signal and the synchronous [FB] clock signal as compared to the detected phase difference." Further, said DLL outputs a reference clock delay signal and a synchronous clock delay signal with a phase difference, which is *the sum of* "[the] phase difference between the reference clock signal and the synchronous clock signal" and "a predetermined phase difference" (to increase a phase difference between the signals applied to a PLL).

Hwang fails to disclose a phase difference which is the sum of "the phase difference between the reference clock and the synchronous clock" and "a predetermined phase difference."

At least for failing to disclose the claim element of a phase difference, which is the sum of "the phase difference between the reference clock and the synchronous clock" and "a predetermined phase difference," the rejection of claim 1 as being anticipated by Hwang under 35 U.S.C. §102(b) should be withdrawn.

Further, *Hwang* fails to disclose a DLL having a phase difference changing means for increasing the phase difference. Assuming only for the sake of argument that the fixed delay in *Hwang* could be analogous to "a predetermined phase difference" of claim 1, *Hwang*'s fixed delay and the variable delay are taught as being designed to decrease the phase difference between the signals applied to the PLL. At least for failing to disclose a phase changing means for increasing the phase difference between the reference clock signal and the synchronous clock signal, the rejection of claim 1 as being anticipated by Hwang under 35 U.S.C. §102(b) should be withdrawn.

Amended claim 8 incorporates subject matter analogous to that discussed above in the traversal of claim 1. In turn, an analogous argument is asserted for the allowability of claim 8. Therefore, the rejection of claim 8 as being anticipated by *Hwang* under 35 U.S.C. §102(b) should be withdrawn.

Claims 3 and 7 are asserted as being allowable at least by virtue of their dependence from an allowable independent claim.

III. Allowable Subject Matter.

Applicant thanks the Examiner for indicating that claims 2, 4-6 and 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. By this Amendment claims 2, 4-6 and 9-11 are presented in independent form as new independent claims 12-18.

In view of the preceding amendments and remarks, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephonic interview, he is kindly requested to contact the undersigned at the local telephone number listed below.

The USPTO is directed and authorized to charge all required fees (except the Issue/Publication Fees) to our Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Amelia F. Morani, Ph.D.
Registration No. 52,049

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: June 8, 2005